



Nuclei RISC-V Processor

NA300 Product Brief

Overall Introduction

Nuclei NA300 is a processor based on RISC-V architecture, which achieves ISO 26262 ASIL-D Ready certificate. The certificate is accomplished together with Exida.

Nuclei NA300 features a 3-stage, dual issue in order pipeline that is compatible with **RV32IMACFDBPC/Zcxlcz**. **NA300** delivers 1.5 Dhrystone/MHz, 3.4 Coremark/MHz.



NA300 supports both instruction and data local memory (**ILM/DLM**) gives better real time processing capability. User can also configure instruction and data cache (**I-Cache/D-Cache**) to improve the performance of the overall subsystem.

NA300 aims for automotive application and is already deployed in **Engine ECU**. NA300 is comparable to ARM Cortex-M33.



Extreme Cost Effective



RV32 IMACFDPB



3-stage Pipeline
Single/Dual Issue
Configurable



Support
I/D-Cache



PMP and TEE
Security Features



Single/Double
Precision FP
and SIMD DSP Unit



ASIL-D Ready



AHB-Lite
System Bus



RISC-V
Standard Debug



4-Wire JTAG
2-Wire JTAG



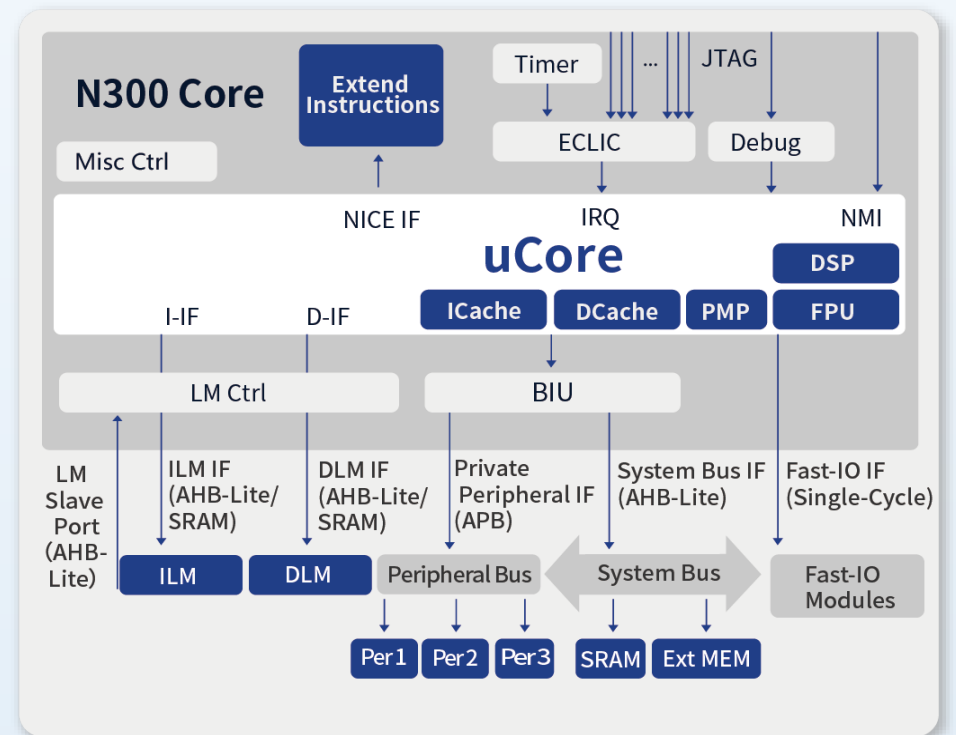
Low Latency
Interrupt



Full Dev Kit & SDK

NA300 Feature

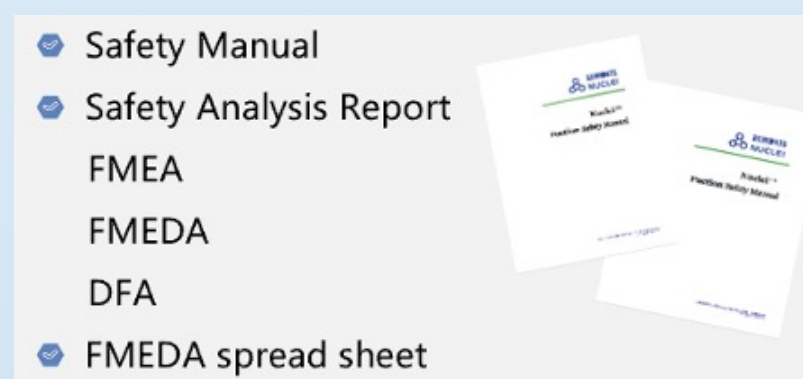
- ISO26262 ASIL-D Ready certified, excellent for Automotive and Functional Safety application;
- RV32IMACFDBPC/Zcxlcz compatible, 3-stage, dual issue in order pipeline;
- Support 32b AHB bus interface, 32b AXI Slave Port and ILM/DLM interface;
- Double/Single Precision floating point and DSP Extension;
- Configurable ILM (Instruction Local Memory) & DLM(Data Local Memory) with ECC;
- Configurable I-Cache & D-Cache with ECC;
- PMP and TEE (Trust Execution Environment) configurable;
- Support standard JTAG & cJTAG interface and Linux/Windows debug tools;
- Support standard RISC-V GNU toolchain and Linux/Windows dev environment (IDE)



NA300 ISO26262 ASIL-D Certificate



NA Series Safety Package



NA300 Memory Subsystem

N300 Series supports local instruction and data memory: **ILM (Instruction Local Memory)** 和 **DLM (Data Local Memory)**, providing real-time processing capability:

- ILM and DLM can be configured from **128B-2GB**, allowing excellent flexibility;
- **AHB-Lite interface and SRAM interface** with customized **address space**.

N300 Series supports Instruction Cache

- **2-way, 32B cache line** structure
- Cache size from **1KB-64KB**
- If ILM is not configured, I-Cache can be configured to **Scratchpad Mode** through CSR
- Support cache line **LOCK and INVAL** operation

N300 Series supports Data Cache

- **2-way, 32B cache line** structure
- Cache size from **1KB-64KB**
- Support cache line **LOCK and INVAL** operation

NA300 System Interface Introduction

Bus Interface	Description	Atomic Support	Burst Support	Cacheability	Protocols	Bus Width
System Bus	System Instruction and Data	Yes	Yes	Configurable	AHB-Lite	32 bit
I-Cache Bus	Used for I-Cache miss	No	Yes	Configurable	AHB-Lite	32 bit
ILM Interface	Local Instruction	No	No	No	SRAM/ AHB-Lite	32 bit
DLM Interface	Local Data	No	No	No	SRAM/ AHB-Lite	32 bit
PPI Interface	Private Peripherals	No	No	No	AHB-Lite	32 bit
Slave Interface	External Master Read	No	No	No	AHB-Lite	32 bit

Nuclei CPU Subsystem

Using internal tools from Nuclei to integrate CPU IPs with other peripheral IPs, verify and deliver a **full subsystem solution** to customer.

- Save money: Full subsystem IP **reduces customer's cost**;
- Save time: Pre-integrated SoC subsystem **saves customer's development cycle**;
- Save effort: Related SoC driver and SDK help **fast prototype bring up**.

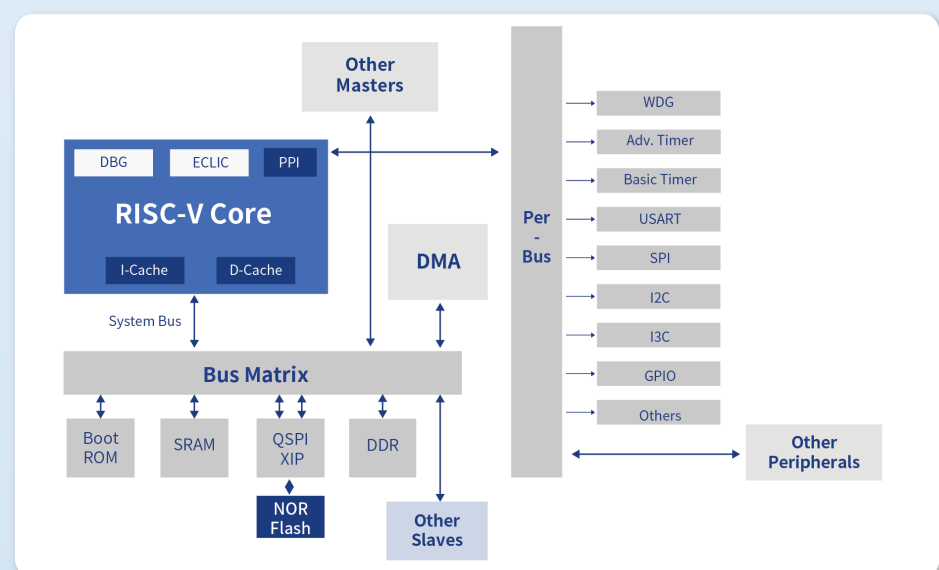


Innovative Subsystem IP Use Case

Use Case #1

Single-core:

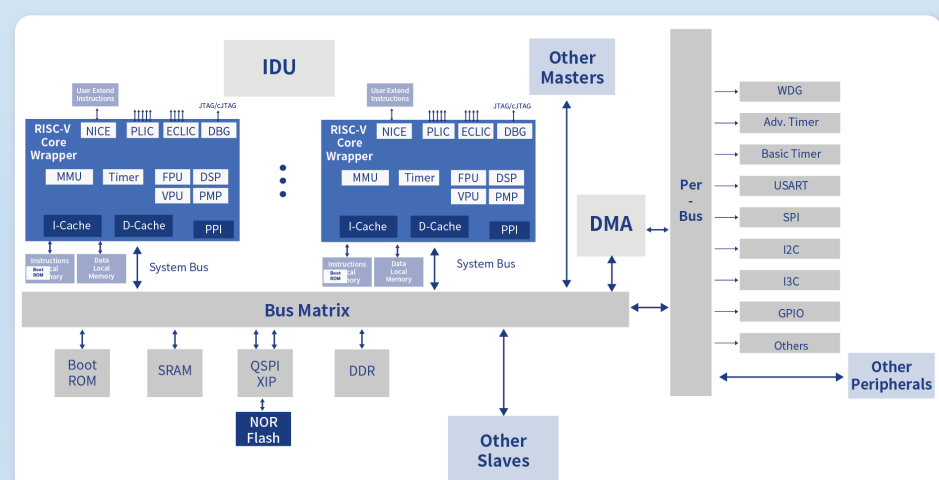
Customer succeeded to **bring up in 2 weeks** based on delivered IP package & SDK



Use Case #2

Multi-core:

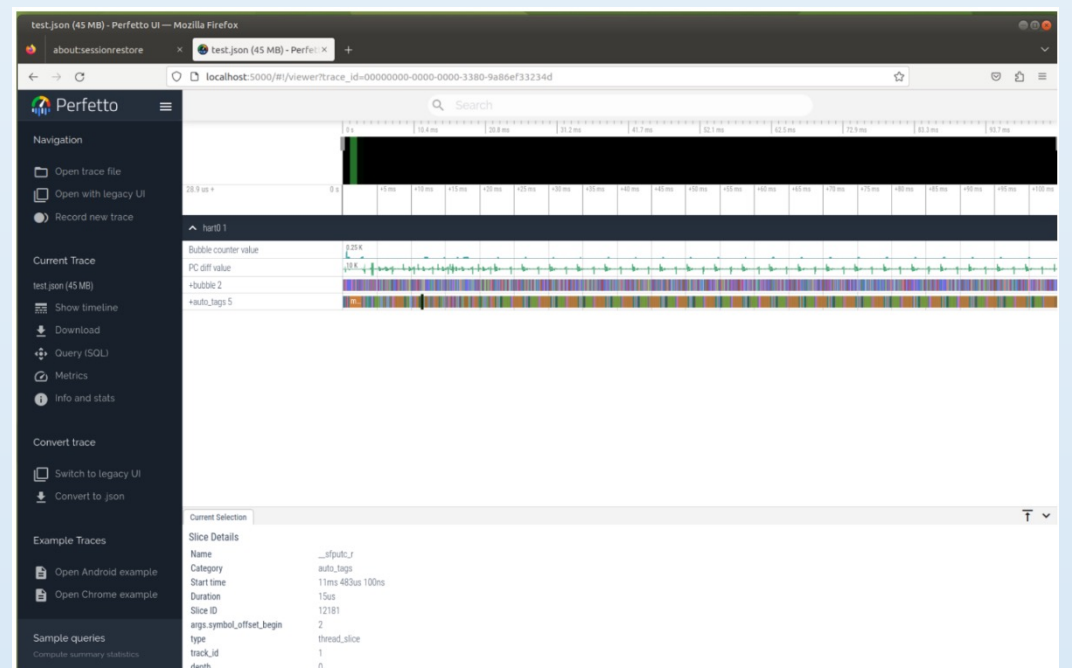
Supported two modes (**real-time & application**), including IDU, bus matrix, etc.



Nuclei IDE

Eclipse CDT Based development environment, easy hands on with manual.

- Nuclei RISC-V GCC, OpenOCD and QEMU integrated
- Nuclei Package(NPK) software solution
- Support SoC Subsystem SDK one-click import
- Portable executables, without installation
- One-click project template
- One-click project configuration
- In system debugging and programming
- Integrated serial port tool
- Real time register display
- Support Linux and Windows
- Deeply integrated with RV Prof – professional performance profiling and optimizing tool, instruction and cycle level accurate
- Embedded with RISC-V e-trace, debug and analyze performance with ATB2AXI module and trace decoder



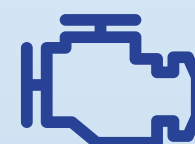
NA300 Has Been Deployed to Automotive Applications



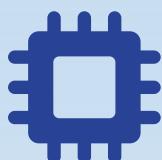
ADAS



Lidar



Engine ECU



MCU



Gateway



Computing