



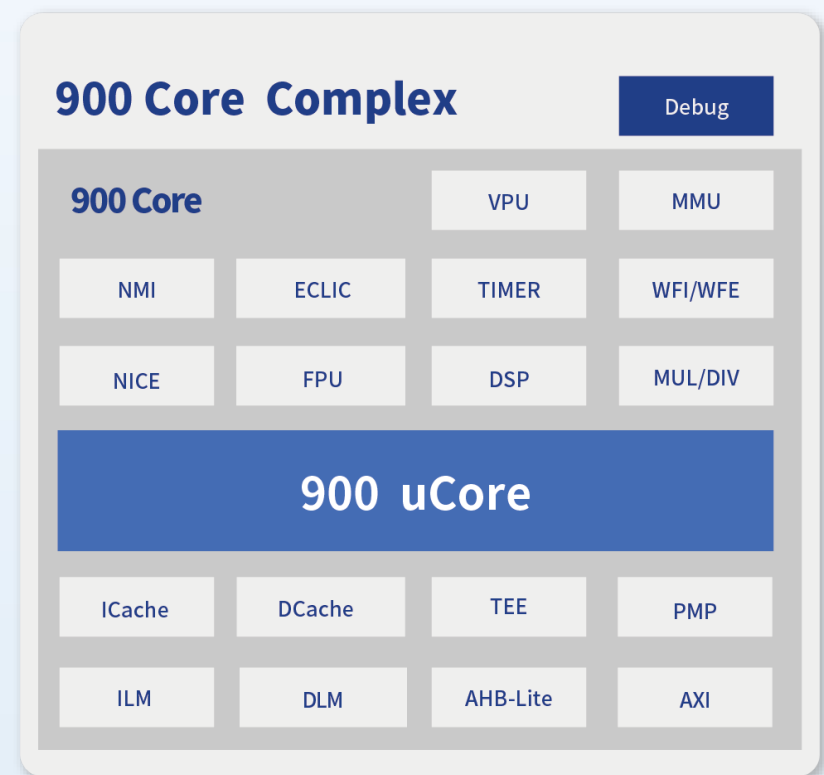
Nuclei RISC-V Processor

NA900 Product Brief

Overall Introduction

Nuclei NA900 is a high-performance processor based on RISC-V architecture. NA900 features a **dual-issue 9-stage in-order execution pipeline**. NA900 is the 1st RISC-V CPU IP that achieves ISO 26262 ASIL-D product certificate. The certificate is accomplished together with Exida.













As a high-performance, **NA900** gives 2.78/5.99(legal/best) Dhrystone/MHz, 5.23 Coremark/MHz.



900 Series supports both instruction and data local memory (**ILM/DLM**) gives better real time processing capability. User can also configure instruction and data cache (**I-Cache/D-Cache**) to improve the performance of the overall subsystem.

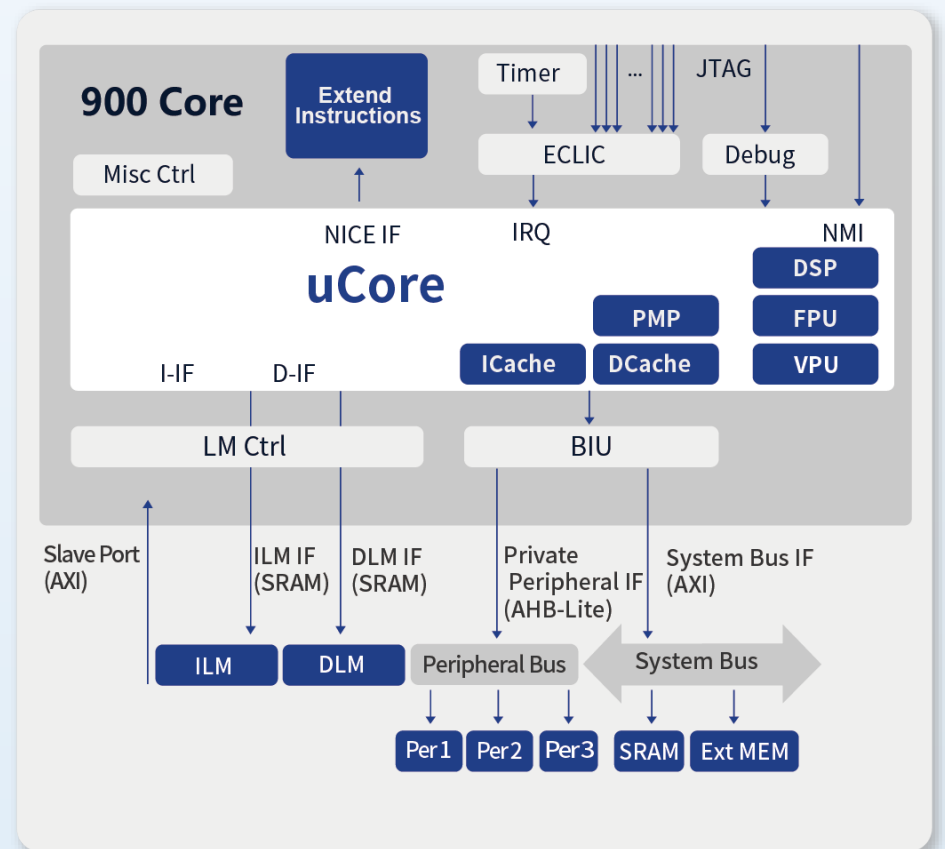
NA900 supports **Dual-Core Lockstep Mode** for ASIL-D functional safety requirement with 99% single point coverage. Meanwhile, NA900 can be configured as **Dual-Core Split Mode**, with each core working separately on ASIL-B level, delivering higher performance. Split Mode **can be configured through software**, giving customer huge flexibility during system level design.

NA900 aims for automotive application and is already deployed in **Engine ECU, ADAS, Gateway and Lidar**. NA900 is comparable to ARM Cortex-R52.

 High Performance Real-time Capability	 RV32/64IMACFDP VBZfh	 9-stage Pipeline	 Support I/DCache	 Machine Mode User Mode Supervisor Mode	 Dual Core Lock Step Dual Core Split
 ASIL-D	 AXI System Bus	 RISC-V Standard Debug	 4-Wire JTAG 2-Wire cJTAG	 Low Latency Interrupt	 Full Dev Kit & SDK

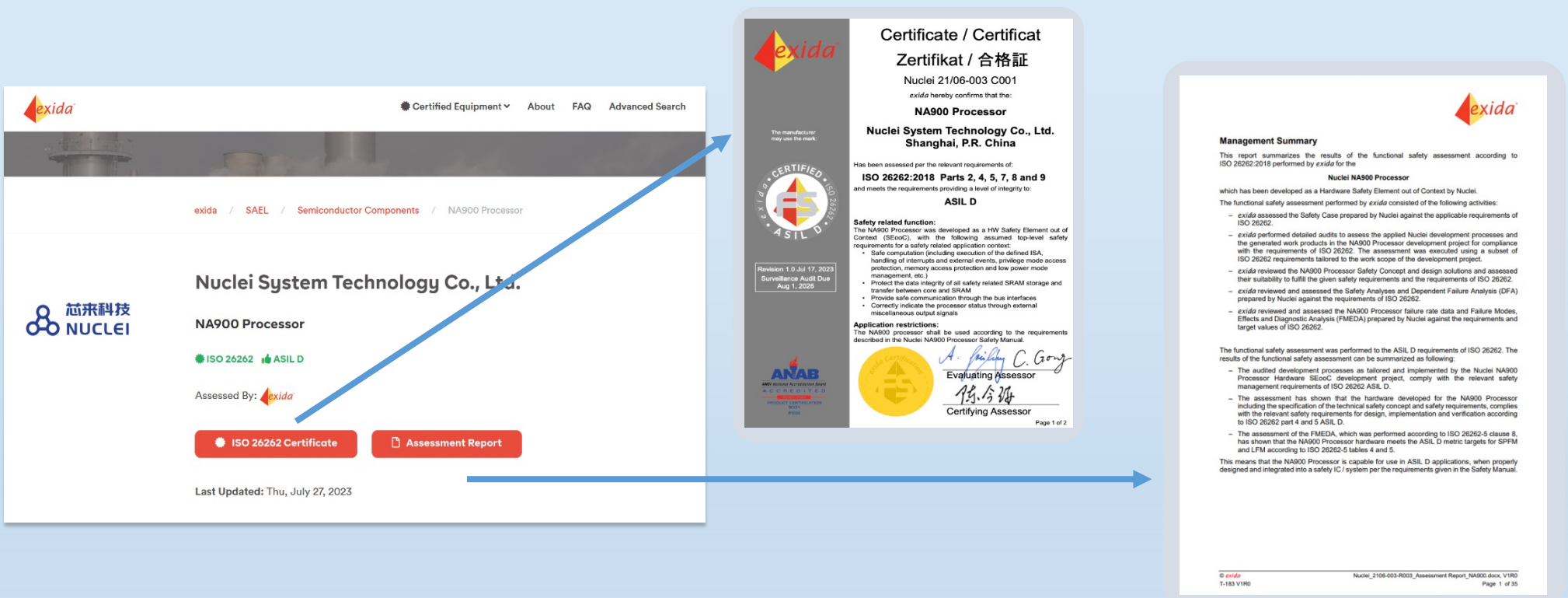
NA900 Feature

- ISO26262 ASIL-D product certified, excellent for Automotive and Functional Safety application;
- RV32IMACFDPB compatible, 9-stage in order **dual-issue** pipeline;
- Support **64b** AXI system interface , 32b AHB-Lite private peripheral interface and ILM/DLM interface;
- **Double/Single Precision** floating point and **DSP** Extension;
- Configurable ILM (**Instruction Local Memory**) & DLM(**Data Local Memory**) with **ECC**;
- Configurable **I-Cache** with Scratchpad mode & **D-Cache** with **ECC**;
- Configurable **PMP** and **TEE (Trust Execution Environment)** for **system security**;
- Support standard **JTAG & cJTAG** interface and Linux/Windows debug tools;
- Support standard RISC-V GNU toolchain and Linux/Windows dev environment (**IDE**)

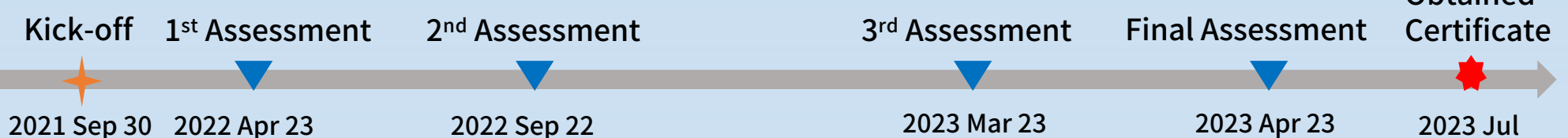


NA900 ISO26262 ASIL-D Certificate and Report

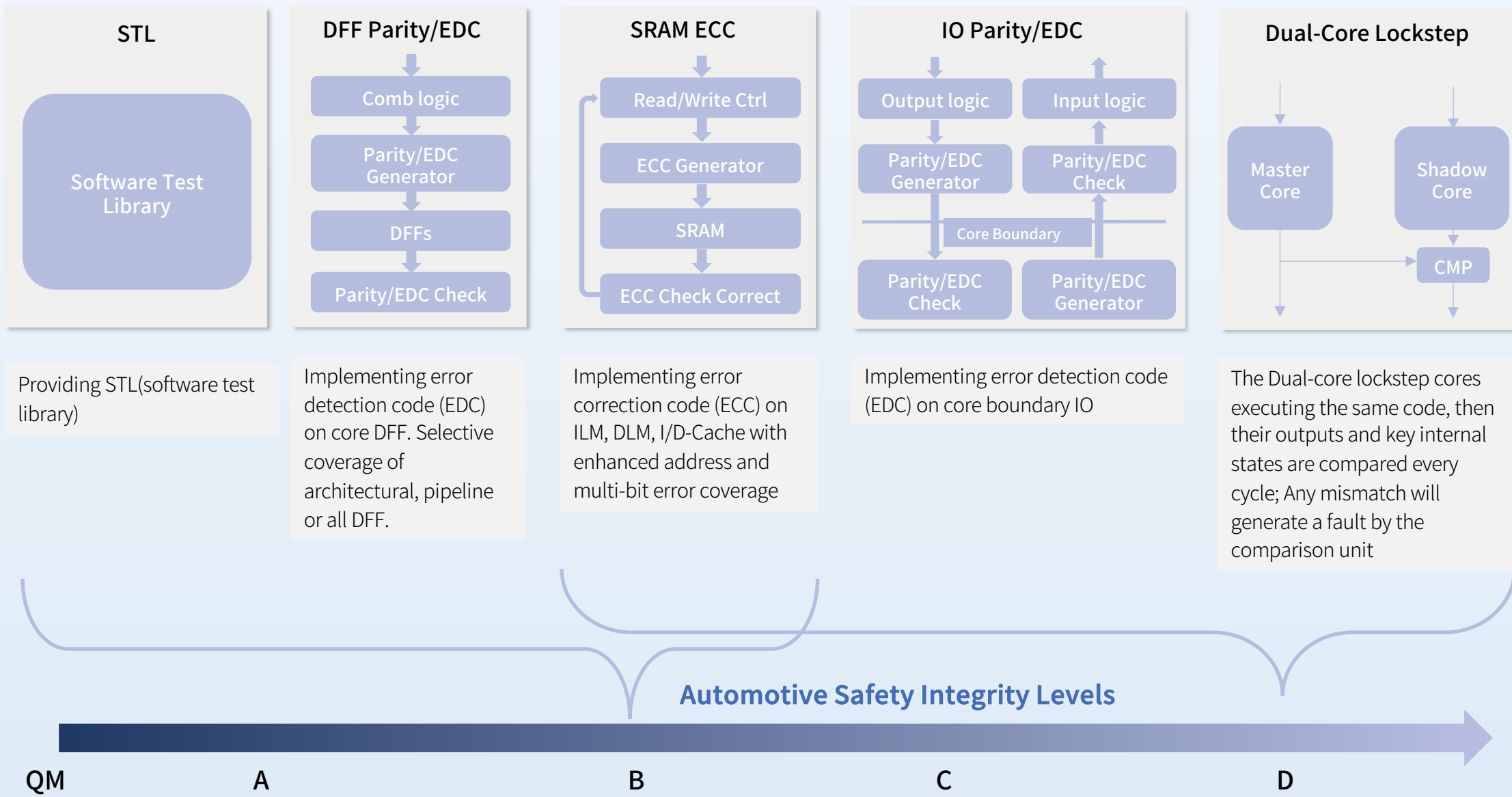
<https://www.exida.com/SAEL-Safety/nuclei-system-technology-co-ltd-na900-processor>



The image shows the Exida website interface for the NA900 Processor certification. The website displays the product name, assessed by Exida, and provides links for the **ISO 26262 Certificate** and **Assessment Report**. The certificate and report are shown as separate documents. The certificate is titled "Certificate / Certificat / Zertifikat / 合格証" and certifies the NA900 Processor for ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9, ASIL D. The report is titled "Management Summary" and provides a detailed overview of the functional safety assessment process.



Functional Safety (ASIL-B & ASIL-D)



Safety Package

FMEDA

Block / Subblock [Drop-down]:	Block / Component	Block / Component Group	High Level Block / Component Group	λ _{permanent} [FIT]	Failure Mode (FM) for the block	FM distribution permanent	FM distribution transient
Master core	master core	-	-	4.7720	All applicable failure mode of computation or communication execution caused by faults in the master core (100) logic	97.0%	99.0%
Master core	master core	-	-	4.7720	Unexpected ECC error detection: 1. Detect error when not expected (false alarm). 2. Not detect a true ECC error.	1.0%	0.5%
Master core	master core	-	-	4.7720	Generate wrong ECC code to the SRAM write data bus	1.1%	1.1%
Master core	master core	-	-	4.7720	Unexpected SBE correction: 1. Do correction on correct data and result in data error. 2. missing a true SBE correction	1.0%	1.0%

Top level safety requirements (TLRS) on IP / IC Level	TLRS short	SPFM	LFM
1 NA900 shall provide the required safe computation	TLRS 01	99.996%	99.784%
2 NA900 shall protect the data integrity of all safety related SRAM Storage and transfer between core and SRAM.	TLRS 02	99.268%	98.885%
3 NA900 shall provide safe communication through the bus interfaces	TLRS 03	99.996%	99.784%
4 NA900 shall be configured through external miscellaneous input signals, and correctly indicate the processor status through external miscellaneous output signals.	TLRS 04	99.996%	99.784%

Safety Manual

- 2.2. SEooC Overview
 - 2.1 2.1. Definition of Components as SEooC
 - 2.2 2.2. Processor Modes
 - 2.3 2.3. Top-Level Safety Requirements
 - 2.3.1 2.3.1. Performance Impact
 - 2.4 2.4. Top-Level Safe States
 - 2.5 2.5. Non-Functional Requirements
 - 2.6 2.6. Constraints and Assumption of Use
- 3.3. Safety Architecture
 - 3.1 3.1. Safety Status and Fault Signals
 - 3.2 3.2. Safety Measures
 - 3.2.1 3.2.1. Detection & Indication and Reaction Time
 - 3.2.2 3.2.2. Internal Safety Mechanism and Design Measures
 - 3.2.2.1 3.2.2.1. Safety Measure 1: HWSM-DCLS
 - 3.2.2.2 3.2.2.2. Safety Measure 2: HWSM-SRAM-PROT
 - 3.2.2.3 3.2.2.3. Safety Measure 3: I/O Protection HWSM-I-PROT, HWSM-O-PROT
 - 3.2.2.4 3.2.2.4. Safety Measure 4: Non safety Isolation HWSM-NSI-ISO
 - 3.2.2.5 3.2.2.5. Safety Measure 5: TSC Comparator HWSM-DCLS-TSC
 - 3.2.3 3.2.3. External Safety Mechanism
 - 3.2.3.1 3.2.3.1. Safety Measure 6: Watchdog Timer HWSM-EXT-WDG
 - 3.2.3.2 3.2.3.2. Safety Measure 7: External Check on Protected Output Signal HWSM-EXT-O-CHECK
 - 3.3 3.3. Assumption of Use for Safety Mechanisms
- 4.4. Integration Requirements
 - 4.1 4.1. IP configuration
 - 4.2 4.2. Configuration Parameters
 - 4.3 4.3. External Hardware Blocks
 - 4.4 4.4. Verification Activities of Integrator
 - 4.5 4.5. Additional Support From Nuclei

NA900 Memory Subsystem

900 Series supports local instruction and data memory: **ILM (Instruction Local Memory)** 和 **DLM (Data Local Memory)**, providing real-time processing capability:

- ILM and DLM can be configured from **128B-2GB**, allowing excellent flexibility;
- **AHB-Lite interface and SRAM interface** with customized **address space**.

900 Series supports Instruction Cache

- **2-way, 64B cache line** structure
- Cache size from **8KB-64KB**
- Support cache line **LOCK and INVAL** operation

900 Series supports Data Cache

- **2-way, 64B cache line** structure
- Cache size from **8KB-64KB**
- Support cache line **LOCK and INVAL** operation

900 Series System Interface Introduction

Bus Interface	Description	Atomic Support	Burst Support	Cacheability	Protocols	Bus Width
System Bus	System Instruction and Data	Yes	Yes	Configurable	AXI4	64 bit
ILM Interface	Local Instruction	No	No	No	SRAM	64 bit
DLM Interface	Local Data	No	No	No	SRAM	2*32 bit
PPI Interface	Private Peripherals	No	No	No	AHB-Lite	32 bit
Slave Interface	External Master Read	No	Yes	No	AXI4	64 bit

Nuclei CPU Subsystem

Using internal tools from Nuclei to integrate CPU IPs with other peripheral IPs, verify and deliver a **full subsystem solution** to customer.

- Save money: Full subsystem IP **reduces customer's cost**;
- Save time: Pre-integrated SoC subsystem **saves customer's development cycle**;
- Save effort: Related SoC driver and SDK help **fast prototype bring up**.

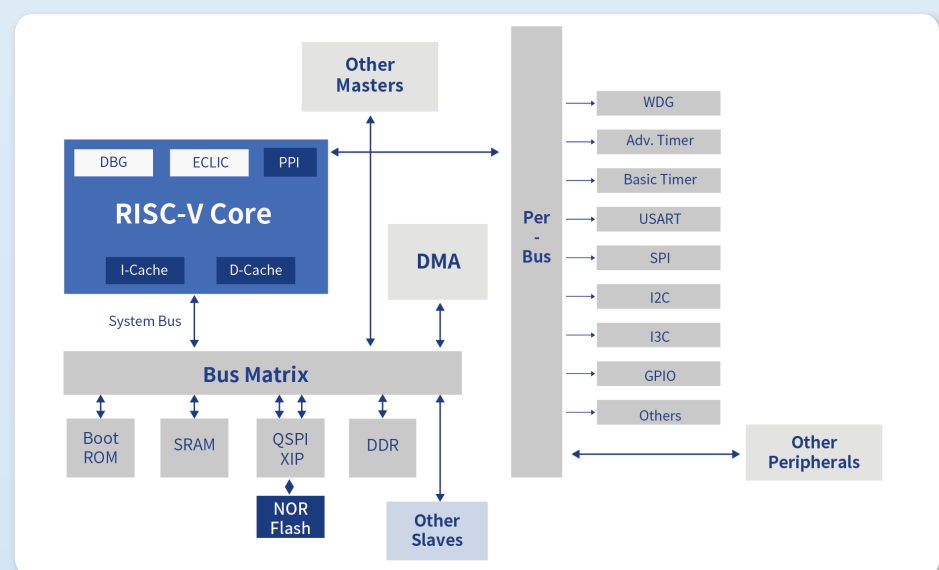


Innovative Subsystem IP Use Case

Use Case #1

Single-core:

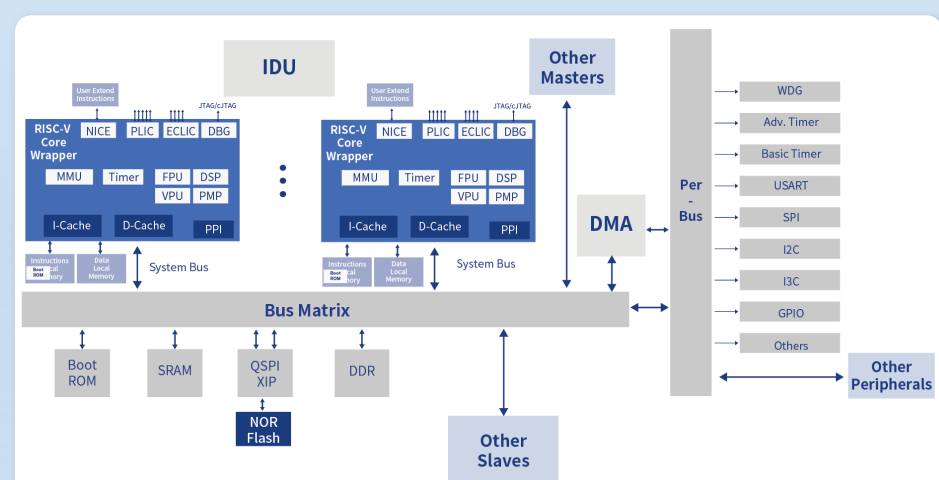
Customer succeeded to **bring up in 2 weeks** based on delivered IP package & SDK



Use Case #2

Multi-core:

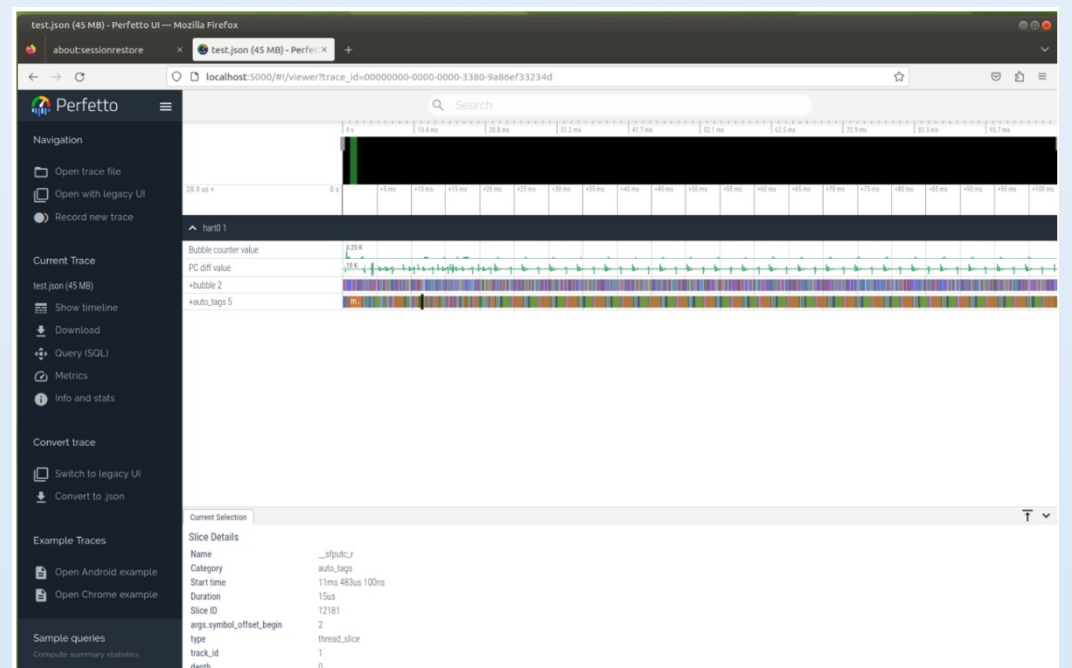
Supported two modes (**real-time & application**), including IDU, bus matrix, etc.



Nuclei IDE

Eclipse CDT Based development environment,
easy hands on with manual.

- Nuclei RISC-V GCC, OpenOCD and QEMU integrated
- Nuclei Package(NPK) software solution
- Support SoC Subsystem SDK one-click import
- Portable executables, without installation
- One-click project template
- One-click project configuration
- In system debugging and programming
- Integrated serial port tool
- Real time register display
- Support Linux and Windows
- Deeply integrated with RV Prof – professional performance profiling and optimizing tool, instruction and cycle level accurate
- Embedded with RISC-V e-trace, debug and analyze performance with ATB2AXI module and trace decoder



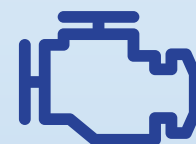
NA900 Series Has Been Deployed to Automotive Applications



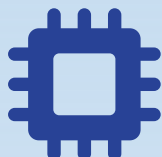
ADAS



Lidar



Engine ECU



MCU



Gateway



Computing