```
set_property CFGBVS VCCO [current_design]

set_property CONFIG_VOLTAGE 3.3 [current_design]


#####              create clock              #####

#set_property -dict { PACKAGE_PIN R4    IOSTANDARD LVDS_25 } [get_ports
{ CLK200MHZ_p }];

#set_property -dict { PACKAGE_PIN T4    IOSTANDARD LVDS_25 } [get_ports
{ CLK200MHZ_n }];

set_property -dict { PACKAGE_PIN W19    IOSTANDARD LVCMOS33 } [get_ports
{ CLK100MHZ }];

set_property -dict { PACKAGE_PIN Y18    IOSTANDARD LVCMOS33 } [get_ports
{ CLK32768KHZ }];

create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports
{CLK100MHZ}];

create_clock -add -name sys_clk_pin -period 30517.58 -waveform {0 15258.79}
[get_ports {CLK32768KHZ}];

#set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets
dut_io_pads_jtag_TCK_i_ival]

set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets IOBUF_jtag_TCK/O]



#####           rst define          #####

set_property PACKAGE_PIN T6  [get_ports fpga_rst  ]

set_property PACKAGE_PIN P20 [get_ports mcu_rst   ]


#####              spi define              #####

set_property PACKAGE_PIN W16 [get_ports  qspi_cs    ]

set_property PACKAGE_PIN W15 [get_ports  qspi_sck   ]

set_property PACKAGE_PIN U16 [get_ports {qspi_dq[3]}]

set_property PACKAGE_PIN T16 [get_ports {qspi_dq[2]}]

set_property PACKAGE_PIN T14 [get_ports {qspi_dq[1]}]

set_property PACKAGE_PIN T15 [get_ports {qspi_dq[0]}]
```

```
#####            MCU JTAG define          #####
set_property PACKAGE_PIN N17 [get_ports mcu_TDO]
set_property PACKAGE_PIN P15 [get_ports mcu_TCK]
set_property PACKAGE_PIN T18 [get_ports mcu_TDI]
set_property PACKAGE_PIN P17 [get_ports mcu_TMS]

#####            PMU define             #####
set_property PACKAGE_PIN U15 [get_ports pmu_paden ]
set_property PACKAGE_PIN V15 [get_ports pmu_padrst]
set_property PACKAGE_PIN N15 [get_ports mcu_wakeup]

#####            gpio define            #####
set_property PACKAGE_PIN W17  [get_ports {gpio[31]}]
set_property PACKAGE_PIN AA18 [get_ports {gpio[30]}]
set_property PACKAGE_PIN AB18 [get_ports {gpio[29]}]
set_property PACKAGE_PIN U17  [get_ports {gpio[28]}]
set_property PACKAGE_PIN U18  [get_ports {gpio[27]}]
set_property PACKAGE_PIN P14  [get_ports {gpio[26]}]
set_property PACKAGE_PIN R14  [get_ports {gpio[25]}]
set_property PACKAGE_PIN R18  [get_ports {gpio[24]}]
set_property PACKAGE_PIN V20  [get_ports {gpio[23]}]
set_property PACKAGE_PIN W20  [get_ports {gpio[22]}]
set_property PACKAGE_PIN Y19  [get_ports {gpio[21]}]
set_property PACKAGE_PIN V18  [get_ports {gpio[20]}]
set_property PACKAGE_PIN V19  [get_ports {gpio[19]}]
set_property PACKAGE_PIN AA19 [get_ports {gpio[18]}]
set_property PACKAGE_PIN R17  [get_ports {gpio[17]}]
set_property PACKAGE_PIN P16  [get_ports {gpio[16]}]
set_property PACKAGE_PIN V22  [get_ports {gpio[15]}]
set_property PACKAGE_PIN T21  [get_ports {gpio[14]}]
```

```
set_property PACKAGE_PIN U21  [get_ports {gpio[13]}]
set_property PACKAGE_PIN P19  [get_ports {gpio[12]}]
set_property PACKAGE_PIN R19  [get_ports {gpio[11]}]
set_property PACKAGE_PIN N13  [get_ports {gpio[10]}]
set_property PACKAGE_PIN T20  [get_ports {gpio[9]}]
set_property PACKAGE_PIN W21  [get_ports {gpio[8]}]
set_property PACKAGE_PIN U20  [get_ports {gpio[7]}]
set_property PACKAGE_PIN AB22 [get_ports {gpio[6]}]
set_property PACKAGE_PIN AB21 [get_ports {gpio[5]}]
set_property PACKAGE_PIN Y22  [get_ports {gpio[4]}]
set_property PACKAGE_PIN Y21  [get_ports {gpio[3]}]
set_property PACKAGE_PIN AA21 [get_ports {gpio[2]}]
set_property PACKAGE_PIN AA20 [get_ports {gpio[1]}]
set_property PACKAGE_PIN W22  [get_ports {gpio[0]}]



#####           clock & rst define          #####
set_property IOSTANDARD LVCMOS15 [get_ports fpga_rst  ]
set_property IOSTANDARD LVCMOS33 [get_ports mcu_rst   ]

#####              spi define              #####
set_property IOSTANDARD LVCMOS33 [get_ports  qspi_cs    ]
set_property IOSTANDARD LVCMOS33 [get_ports  qspi_sck   ]
set_property IOSTANDARD LVCMOS33 [get_ports {qspi_dq[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {qspi_dq[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {qspi_dq[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {qspi_dq[0]}]
```

```
#####            MCU JTAG define          #####
set_property IOSTANDARD LVCMOS33 [get_ports mcu_TDO]
set_property IOSTANDARD LVCMOS33 [get_ports mcu_TCK]
set_property IOSTANDARD LVCMOS33 [get_ports mcu_TDI]
set_property IOSTANDARD LVCMOS33 [get_ports mcu_TMS]

#####            PMU define             #####
set_property IOSTANDARD LVCMOS33 [get_ports pmu_paden ]
set_property IOSTANDARD LVCMOS33 [get_ports pmu_padrst]
set_property IOSTANDARD LVCMOS33 [get_ports mcu_wakeup]

#####            gpio define            #####
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[31]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[30]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[29]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[28]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[27]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[26]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[25]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[24]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[23]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[22]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[21]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[20]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[19]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[18]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[17]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[16]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[15]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[14]}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[13]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[12]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[11]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[10]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[9]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[8]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {gpio[0]}]

####FPGA GPIO

#####             BANK13 IO define        #####
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP1]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN1]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP2]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN2]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP3]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN3]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP4]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN4]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP5]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN5]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP6]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN6]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP7]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN7]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP8]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN8]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP9]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN9]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP10]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN10]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP11]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN11]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP12]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN12]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LP13]
set_property IOSTANDARD LVCMOS33 [get_ports B13_LN13]

#####              BANK13 IO define       #####
set_property PACKAGE_PIN Y16   [get_ports B13_LP1]
set_property PACKAGE_PIN AA16  [get_ports B13_LN1]
set_property PACKAGE_PIN AB16  [get_ports B13_LP2]
set_property PACKAGE_PIN AB17  [get_ports B13_LN2]
set_property PACKAGE_PIN AA13  [get_ports B13_LP3]
set_property PACKAGE_PIN AB13  [get_ports B13_LN3]
set_property PACKAGE_PIN AA15  [get_ports B13_LP4]
set_property PACKAGE_PIN AB15  [get_ports B13_LN4]
set_property PACKAGE_PIN Y13   [get_ports B13_LP5]
set_property PACKAGE_PIN AA14  [get_ports B13_LN5]
set_property PACKAGE_PIN W14   [get_ports B13_LP6]
set_property PACKAGE_PIN Y14   [get_ports B13_LN6]
```

```
set_property PACKAGE_PIN AB11  [get_ports B13_LP7]
set_property PACKAGE_PIN AB12  [get_ports B13_LN7]
set_property PACKAGE_PIN AA9   [get_ports B13_LP8]
set_property PACKAGE_PIN AB10  [get_ports B13_LN8]
set_property PACKAGE_PIN AA10  [get_ports B13_LP9]
set_property PACKAGE_PIN AA11  [get_ports B13_LN9]
set_property PACKAGE_PIN V10   [get_ports B13_LP10]
set_property PACKAGE_PIN W10   [get_ports B13_LN10]
set_property PACKAGE_PIN Y11   [get_ports B13_LP11]
set_property PACKAGE_PIN Y12   [get_ports B13_LN11]
set_property PACKAGE_PIN W11   [get_ports B13_LP12]
set_property PACKAGE_PIN W12   [get_ports B13_LN12]
set_property PACKAGE_PIN V13   [get_ports B13_LP13]
set_property PACKAGE_PIN V14  [get_ports B13_LN13]

#####              BANK15 IO define         #####
set_property IOSTANDARD LVCMOS18 [get_ports B15_IO0]
set_property IOSTANDARD LVDS     [get_ports B15_LP1]
set_property IOSTANDARD LVDS     [get_ports B15_LN1]
set_property IOSTANDARD LVDS     [get_ports B15_LP2]
set_property IOSTANDARD LVDS     [get_ports B15_LN2]
set_property IOSTANDARD LVDS     [get_ports B15_LP3]
set_property IOSTANDARD LVDS     [get_ports B15_LN3]
set_property IOSTANDARD LVDS     [get_ports B15_LP4]
set_property IOSTANDARD LVDS     [get_ports B15_LN4]
set_property IOSTANDARD LVDS     [get_ports B15_LP5]
set_property IOSTANDARD LVDS     [get_ports B15_LN5]
set_property IOSTANDARD LVDS     [get_ports B15_LP6]
set_property IOSTANDARD LVDS     [get_ports B15_LN6]
set_property IOSTANDARD LVDS     [get_ports B15_LP7]
```

```
set_property IOSTANDARD LVDS    [get_ports B15_LN7]
set_property IOSTANDARD LVDS    [get_ports B15_LP8]
set_property IOSTANDARD LVDS    [get_ports B15_LN8]
set_property IOSTANDARD LVDS    [get_ports B15_LP9]
set_property IOSTANDARD LVDS    [get_ports B15_LN9]
set_property IOSTANDARD LVDS    [get_ports B15_LP10]
set_property IOSTANDARD LVDS    [get_ports B15_LN10]
set_property IOSTANDARD LVDS    [get_ports B15_LP11]
set_property IOSTANDARD LVDS    [get_ports B15_LN11]
set_property IOSTANDARD LVDS    [get_ports B15_LP12]
set_property IOSTANDARD LVDS    [get_ports B15_LN12]
set_property IOSTANDARD LVDS    [get_ports B15_LP13]
set_property IOSTANDARD LVDS    [get_ports B15_LN13]
set_property IOSTANDARD LVDS    [get_ports B15_LP14]
set_property IOSTANDARD LVDS    [get_ports B15_LN14]
set_property IOSTANDARD LVDS    [get_ports B15_LP15]
set_property IOSTANDARD LVDS    [get_ports B15_LN15]
set_property IOSTANDARD LVDS    [get_ports B15_LP16]
set_property IOSTANDARD LVDS    [get_ports B15_LN16]
set_property IOSTANDARD LVDS    [get_ports B15_LP17]
set_property IOSTANDARD LVDS    [get_ports B15_LN17]
set_property IOSTANDARD LVDS    [get_ports B15_LP18]
set_property IOSTANDARD LVDS    [get_ports B15_LN18]
set_property IOSTANDARD LVDS    [get_ports B15_LP19]
set_property IOSTANDARD LVDS    [get_ports B15_LN19]
set_property IOSTANDARD LVDS    [get_ports B15_LP20]
set_property IOSTANDARD LVDS    [get_ports B15_LN20]
set_property IOSTANDARD LVDS    [get_ports B15_LP21]
set_property IOSTANDARD LVDS    [get_ports B15_LN21]
set_property IOSTANDARD LVDS    [get_ports B15_LP22]
```

```
set_property IOSTANDARD LVDS     [get_ports B15_LN22]
set_property IOSTANDARD LVDS     [get_ports B15_LP23]
set_property IOSTANDARD LVDS     [get_ports B15_LN23]
set_property IOSTANDARD LVDS     [get_ports B15_LP24]
set_property IOSTANDARD LVDS     [get_ports B15_LN24]
set_property IOSTANDARD LVCMOS18 [get_ports B15_IO25]

#####              BANK15 IO define       #####
set_property PACKAGE_PIN J16  [get_ports B15_IO0]
set_property PACKAGE_PIN H13  [get_ports B15_LP1]
set_property PACKAGE_PIN G13  [get_ports B15_LN1]
set_property PACKAGE_PIN G15  [get_ports B15_LP2]
set_property PACKAGE_PIN G16  [get_ports B15_LN2]
set_property PACKAGE_PIN J14  [get_ports B15_LP3]
set_property PACKAGE_PIN H14  [get_ports B15_LN3]
set_property PACKAGE_PIN G17  [get_ports B15_LP4]
set_property PACKAGE_PIN G18  [get_ports B15_LN4]
set_property PACKAGE_PIN J15  [get_ports B15_LP5]
set_property PACKAGE_PIN H15  [get_ports B15_LN5]
set_property PACKAGE_PIN H17  [get_ports B15_LP6]
set_property PACKAGE_PIN H18  [get_ports B15_LN6]
set_property PACKAGE_PIN J22  [get_ports B15_LP7]
set_property PACKAGE_PIN H22  [get_ports B15_LN7]
set_property PACKAGE_PIN H20  [get_ports B15_LP8]
set_property PACKAGE_PIN G20  [get_ports B15_LN8]
set_property PACKAGE_PIN K21  [get_ports B15_LP9]
set_property PACKAGE_PIN K22  [get_ports B15_LN9]
set_property PACKAGE_PIN M21  [get_ports B15_LP10]
set_property PACKAGE_PIN L21  [get_ports B15_LN10]
set_property PACKAGE_PIN J20  [get_ports B15_LP11]
```

```
set_property PACKAGE_PIN J21  [get_ports B15_LN11]
set_property PACKAGE_PIN J19  [get_ports B15_LP12]
set_property PACKAGE_PIN H19  [get_ports B15_LN12]
set_property PACKAGE_PIN K18  [get_ports B15_LP13]
set_property PACKAGE_PIN K19  [get_ports B15_LN13]
set_property PACKAGE_PIN L19  [get_ports B15_LP14]
set_property PACKAGE_PIN L20  [get_ports B15_LN14]
set_property PACKAGE_PIN N22  [get_ports B15_LP15]
set_property PACKAGE_PIN M22  [get_ports B15_LN15]
set_property PACKAGE_PIN M18  [get_ports B15_LP16]
set_property PACKAGE_PIN L18  [get_ports B15_LN16]
set_property PACKAGE_PIN N18  [get_ports B15_LP17]
set_property PACKAGE_PIN N19  [get_ports B15_LN17]
set_property PACKAGE_PIN N20  [get_ports B15_LP18]
set_property PACKAGE_PIN M20  [get_ports B15_LN18]
set_property PACKAGE_PIN K13  [get_ports B15_LP19]
set_property PACKAGE_PIN K14  [get_ports B15_LN19]
set_property PACKAGE_PIN M13  [get_ports B15_LP20]
set_property PACKAGE_PIN L13  [get_ports B15_LN20]
set_property PACKAGE_PIN K17  [get_ports B15_LP21]
set_property PACKAGE_PIN J17  [get_ports B15_LN21]
set_property PACKAGE_PIN L14  [get_ports B15_LP22]
set_property PACKAGE_PIN L15  [get_ports B15_LN22]
set_property PACKAGE_PIN L16  [get_ports B15_LP23]
set_property PACKAGE_PIN K16  [get_ports B15_LN23]
set_property PACKAGE_PIN M15  [get_ports B15_LP24]
set_property PACKAGE_PIN M16  [get_ports B15_LN24]
set_property PACKAGE_PIN M17  [get_ports B15_IO25]

#####            BANK16 IO define        #####
```

```
set_property IOSTANDARD LVCMOS18 [get_ports B16_IO0]
set_property IOSTANDARD LVDS     [get_ports B16_LP1]
set_property IOSTANDARD LVDS     [get_ports B16_LN1]
set_property IOSTANDARD LVDS     [get_ports B16_LP2]
set_property IOSTANDARD LVDS     [get_ports B16_LN2]
set_property IOSTANDARD LVDS     [get_ports B16_LP3]
set_property IOSTANDARD LVDS     [get_ports B16_LN3]
set_property IOSTANDARD LVDS     [get_ports B16_LP4]
set_property IOSTANDARD LVDS     [get_ports B16_LN4]
set_property IOSTANDARD LVDS     [get_ports B16_LP5]
set_property IOSTANDARD LVDS     [get_ports B16_LN5]
set_property IOSTANDARD LVDS     [get_ports B16_LP6]
set_property IOSTANDARD LVDS     [get_ports B16_LN6]
set_property IOSTANDARD LVDS     [get_ports B16_LP7]
set_property IOSTANDARD LVDS     [get_ports B16_LN7]
set_property IOSTANDARD LVDS     [get_ports B16_LP8]
set_property IOSTANDARD LVDS     [get_ports B16_LN8]
set_property IOSTANDARD LVDS     [get_ports B16_LP9]
set_property IOSTANDARD LVDS     [get_ports B16_LN9]
set_property IOSTANDARD LVDS     [get_ports B16_LP10]
set_property IOSTANDARD LVDS     [get_ports B16_LN10]
set_property IOSTANDARD LVDS     [get_ports B16_LP11]
set_property IOSTANDARD LVDS     [get_ports B16_LN11]
set_property IOSTANDARD LVDS     [get_ports B16_LP12]
set_property IOSTANDARD LVDS     [get_ports B16_LN12]
set_property IOSTANDARD LVDS     [get_ports B16_LP13]
set_property IOSTANDARD LVDS     [get_ports B16_LN13]
set_property IOSTANDARD LVDS     [get_ports B16_LP14]
set_property IOSTANDARD LVDS     [get_ports B16_LN14]
set_property IOSTANDARD LVDS     [get_ports B16_LP15]
```

```
set_property IOSTANDARD LVDS     [get_ports B16_LN15]
set_property IOSTANDARD LVDS     [get_ports B16_LP16]
set_property IOSTANDARD LVDS     [get_ports B16_LN16]
set_property IOSTANDARD LVDS     [get_ports B16_LP17]
set_property IOSTANDARD LVDS     [get_ports B16_LN17]
set_property IOSTANDARD LVDS     [get_ports B16_LP18]
set_property IOSTANDARD LVDS     [get_ports B16_LN18]
set_property IOSTANDARD LVDS     [get_ports B16_LP19]
set_property IOSTANDARD LVDS     [get_ports B16_LN19]
set_property IOSTANDARD LVDS     [get_ports B16_LP20]
set_property IOSTANDARD LVDS     [get_ports B16_LN20]
set_property IOSTANDARD LVDS     [get_ports B16_LP21]
set_property IOSTANDARD LVDS     [get_ports B16_LN21]
set_property IOSTANDARD LVDS     [get_ports B16_LP22]
set_property IOSTANDARD LVDS     [get_ports B16_LN22]
set_property IOSTANDARD LVDS     [get_ports B16_LP23]
set_property IOSTANDARD LVDS     [get_ports B16_LN23]
set_property IOSTANDARD LVDS     [get_ports B16_LP24]
set_property IOSTANDARD LVDS     [get_ports B16_LN24]
set_property IOSTANDARD LVCMOS18 [get_ports B16_IO25]

#####              BANK16 IO define       #####
set_property PACKAGE_PIN F15  [get_ports B16_IO0]
set_property PACKAGE_PIN F13  [get_ports B16_LP1]
set_property PACKAGE_PIN F14  [get_ports B16_LN1]
set_property PACKAGE_PIN F16  [get_ports B16_LP2]
set_property PACKAGE_PIN E17  [get_ports B16_LN2]
set_property PACKAGE_PIN C14  [get_ports B16_LP3]
set_property PACKAGE_PIN C15  [get_ports B16_LN3]
set_property PACKAGE_PIN E13  [get_ports B16_LP4]
```

```
set_property PACKAGE_PIN E14  [get_ports B16_LN4]
set_property PACKAGE_PIN E16  [get_ports B16_LP5]
set_property PACKAGE_PIN D16  [get_ports B16_LN5]
set_property PACKAGE_PIN D14  [get_ports B16_LP6]
set_property PACKAGE_PIN D15  [get_ports B16_LN6]
set_property PACKAGE_PIN B15  [get_ports B16_LP7]
set_property PACKAGE_PIN B16  [get_ports B16_LN7]
set_property PACKAGE_PIN C13  [get_ports B16_LP8]
set_property PACKAGE_PIN B13  [get_ports B16_LN8]
set_property PACKAGE_PIN A15  [get_ports B16_LP9]
set_property PACKAGE_PIN A16  [get_ports B16_LN9]
set_property PACKAGE_PIN A13  [get_ports B16_LP10]
set_property PACKAGE_PIN A14  [get_ports B16_LN10]
set_property PACKAGE_PIN B17  [get_ports B16_LP11]
set_property PACKAGE_PIN B18  [get_ports B16_LN11]
set_property PACKAGE_PIN D17  [get_ports B16_LP12]
set_property PACKAGE_PIN C17  [get_ports B16_LN12]
set_property PACKAGE_PIN C18  [get_ports B16_LP13]
set_property PACKAGE_PIN C19  [get_ports B16_LN13]
set_property PACKAGE_PIN E19  [get_ports B16_LP14]
set_property PACKAGE_PIN D19  [get_ports B16_LN14]
set_property PACKAGE_PIN F18  [get_ports B16_LP15]
set_property PACKAGE_PIN E18  [get_ports B16_LN15]
set_property PACKAGE_PIN B20  [get_ports B16_LP16]
set_property PACKAGE_PIN A20  [get_ports B16_LN16]
set_property PACKAGE_PIN A18  [get_ports B16_LP17]
set_property PACKAGE_PIN A19  [get_ports B16_LN17]
set_property PACKAGE_PIN F19  [get_ports B16_LP18]
set_property PACKAGE_PIN F20  [get_ports B16_LN18]
set_property PACKAGE_PIN D20  [get_ports B16_LP19]
```

```
set_property PACKAGE_PIN C20  [get_ports B16_LN19]
set_property PACKAGE_PIN C22  [get_ports B16_LP20]
set_property PACKAGE_PIN B22  [get_ports B16_LN20]
set_property PACKAGE_PIN B21  [get_ports B16_LP21]
set_property PACKAGE_PIN A21  [get_ports B16_LN21]
set_property PACKAGE_PIN E22  [get_ports B16_LP22]
set_property PACKAGE_PIN D22  [get_ports B16_LN22]
set_property PACKAGE_PIN E21  [get_ports B16_LP23]
set_property PACKAGE_PIN D21  [get_ports B16_LN23]
set_property PACKAGE_PIN G21  [get_ports B16_LP24]
set_property PACKAGE_PIN G22  [get_ports B16_LN24]
set_property PACKAGE_PIN F21  [get_ports B16_IO25]



#####              DDR3 IO define      #####
# PadFunction: IO_L2P_T0_AD12P_35
set_property SLEW FAST [get_ports {DDR3_D[0]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[0]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[0]}]
set_property PACKAGE_PIN C2 [get_ports {DDR3_D[0]}]

# PadFunction: IO_L5P_T0_AD13P_35
set_property SLEW FAST [get_ports {DDR3_D[1]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[1]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[1]}]
set_property PACKAGE_PIN G1 [get_ports {DDR3_D[1]}]

# PadFunction: IO_L1N_T0_AD4N_35
set_property SLEW FAST [get_ports {DDR3_D[2]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[2]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[2]}]
set_property PACKAGE_PIN A1 [get_ports {DDR3_D[2]}]

# PadFunction: IO_L6P_T0_35
set_property SLEW FAST [get_ports {DDR3_D[3]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[3]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[3]}]
set_property PACKAGE_PIN F3 [get_ports {DDR3_D[3]}]

# PadFunction: IO_L2N_T0_AD12N_35
set_property SLEW FAST [get_ports {DDR3_D[4]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[4]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[4]}]
set_property PACKAGE_PIN B2 [get_ports {DDR3_D[4]}]

# PadFunction: IO_L5N_T0_AD13N_35
set_property SLEW FAST [get_ports {DDR3_D[5]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[5]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[5]}]
set_property PACKAGE_PIN F1 [get_ports {DDR3_D[5]}]

# PadFunction: IO_L1P_T0_AD4P_35
set_property SLEW FAST [get_ports {DDR3_D[6]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[6]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[6]}]
set_property PACKAGE_PIN B1 [get_ports {DDR3_D[6]}]

# PadFunction: IO_L4P_T0_35
set_property SLEW FAST [get_ports {DDR3_D[7]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[7]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[7]}]
set_property PACKAGE_PIN E2 [get_ports {DDR3_D[7]}]

# PadFunction: IO_L11P_T1_SRCC_35
set_property SLEW FAST [get_ports {DDR3_D[8]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[8]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[8]}]
set_property PACKAGE_PIN H3 [get_ports {DDR3_D[8]}]

# PadFunction: IO_L11N_T1_SRCC_35
set_property SLEW FAST [get_ports {DDR3_D[9]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[9]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[9]}]
set_property PACKAGE_PIN G3 [get_ports {DDR3_D[9]}]

# PadFunction: IO_L8P_T1_AD14P_35
set_property SLEW FAST [get_ports {DDR3_D[10]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[10]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[10]}]
set_property PACKAGE_PIN H2 [get_ports {DDR3_D[10]}]

# PadFunction: IO_L10N_T1_AD15N_35
set_property SLEW FAST [get_ports {DDR3_D[11]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[11]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[11]}]
set_property PACKAGE_PIN H5 [get_ports {DDR3_D[11]}]

# PadFunction: IO_L7N_T1_AD6N_35
set_property SLEW FAST [get_ports {DDR3_D[12]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[12]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[12]}]
set_property PACKAGE_PIN J1 [get_ports {DDR3_D[12]}]

# PadFunction: IO_L10P_T1_AD15P_35
set_property SLEW FAST [get_ports {DDR3_D[13]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[13]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[13]}]
set_property PACKAGE_PIN J5 [get_ports {DDR3_D[13]}]

# PadFunction: IO_L7P_T1_AD6P_35
set_property SLEW FAST [get_ports {DDR3_D[14]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[14]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[14]}]
set_property PACKAGE_PIN K1 [get_ports {DDR3_D[14]}]

# PadFunction: IO_L12P_T1_MRCC_35
set_property SLEW FAST [get_ports {DDR3_D[15]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[15]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[15]}]
set_property PACKAGE_PIN H4 [get_ports {DDR3_D[15]}]

# PadFunction: IO_L18N_T2_35
set_property SLEW FAST [get_ports {DDR3_D[16]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[16]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[16]}]
set_property PACKAGE_PIN L4 [get_ports {DDR3_D[16]}]

# PadFunction: IO_L16P_T2_35
set_property SLEW FAST [get_ports {DDR3_D[17]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[17]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[17]}]
set_property PACKAGE_PIN M3 [get_ports {DDR3_D[17]}]

# PadFunction: IO_L14P_T2_SRCC_35
set_property SLEW FAST [get_ports {DDR3_D[18]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[18]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[18]}]
set_property PACKAGE_PIN L3 [get_ports {DDR3_D[18]}]

# PadFunction: IO_L17N_T2_35
set_property SLEW FAST [get_ports {DDR3_D[19]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[19]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[19]}]
set_property PACKAGE_PIN J6 [get_ports {DDR3_D[19]}]

# PadFunction: IO_L14N_T2_SRCC_35
set_property SLEW FAST [get_ports {DDR3_D[20]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[20]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[20]}]
set_property PACKAGE_PIN K3 [get_ports {DDR3_D[20]}]

# PadFunction: IO_L17P_T2_35
set_property SLEW FAST [get_ports {DDR3_D[21]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[21]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[21]}]
set_property PACKAGE_PIN K6 [get_ports {DDR3_D[21]}]

# PadFunction: IO_L13N_T2_MRCC_35
set_property SLEW FAST [get_ports {DDR3_D[22]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[22]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[22]}]
set_property PACKAGE_PIN J4 [get_ports {DDR3_D[22]}]

# PadFunction: IO_L18P_T2_35
set_property SLEW FAST [get_ports {DDR3_D[23]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[23]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[23]}]
set_property PACKAGE_PIN L5 [get_ports {DDR3_D[23]}]

# PadFunction: IO_L20N_T3_35
set_property SLEW FAST [get_ports {DDR3_D[24]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[24]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[24]}]
set_property PACKAGE_PIN P1 [get_ports {DDR3_D[24]}]

# PadFunction: IO_L19P_T3_35
set_property SLEW FAST [get_ports {DDR3_D[25]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[25]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[25]}]
set_property PACKAGE_PIN N4 [get_ports {DDR3_D[25]}]

# PadFunction: IO_L20P_T3_35
set_property SLEW FAST [get_ports {DDR3_D[26]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[26]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[26]}]
set_property PACKAGE_PIN R1 [get_ports {DDR3_D[26]}]

# PadFunction: IO_L22N_T3_35
set_property SLEW FAST [get_ports {DDR3_D[27]}]
```

```
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[27]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[27]}]
set_property PACKAGE_PIN N2 [get_ports {DDR3_D[27]}]

# PadFunction: IO_L23P_T3_35
set_property SLEW FAST [get_ports {DDR3_D[28]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[28]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[28]}]
set_property PACKAGE_PIN M6 [get_ports {DDR3_D[28]}]

# PadFunction: IO_L24N_T3_35
set_property SLEW FAST [get_ports {DDR3_D[29]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[29]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[29]}]
set_property PACKAGE_PIN N5 [get_ports {DDR3_D[29]}]

# PadFunction: IO_L24P_T3_35
set_property SLEW FAST [get_ports {DDR3_D[30]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[30]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[30]}]
set_property PACKAGE_PIN P6 [get_ports {DDR3_D[30]}]

# PadFunction: IO_L22P_T3_35
set_property SLEW FAST [get_ports {DDR3_D[31]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_D[31]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_D[31]}]
set_property PACKAGE_PIN P2 [get_ports {DDR3_D[31]}]

# PadFunction: IO_L6N_T0_VREF_34
set_property SLEW FAST [get_ports {DDR3_A[14]}]
```

```
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[14]}]
set_property PACKAGE_PIN V3 [get_ports {DDR3_A[14]}]

# PadFunction: IO_L1N_T0_34
set_property SLEW FAST [get_ports {DDR3_A[13]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[13]}]
set_property PACKAGE_PIN U1 [get_ports {DDR3_A[13]}]

# PadFunction: IO_L4N_T0_34
set_property SLEW FAST [get_ports {DDR3_A[12]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[12]}]
set_property PACKAGE_PIN Y2 [get_ports {DDR3_A[12]}]

# PadFunction: IO_L4P_T0_34
set_property SLEW FAST [get_ports {DDR3_A[11]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[11]}]
set_property PACKAGE_PIN W2 [get_ports {DDR3_A[11]}]

# PadFunction: IO_L5N_T0_34
set_property SLEW FAST [get_ports {DDR3_A[10]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[10]}]
set_property PACKAGE_PIN Y1 [get_ports {DDR3_A[10]}]

# PadFunction: IO_L2P_T0_34
set_property SLEW FAST [get_ports {DDR3_A[9]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[9]}]
set_property PACKAGE_PIN U2 [get_ports {DDR3_A[9]}]

# PadFunction: IO_L2N_T0_34
set_property SLEW FAST [get_ports {DDR3_A[8]}]
```

```
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[8]}]
set_property PACKAGE_PIN V2 [get_ports {DDR3_A[8]}]

# PadFunction: IO_L1P_T0_34
set_property SLEW FAST [get_ports {DDR3_A[7]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[7]}]
set_property PACKAGE_PIN T1 [get_ports {DDR3_A[7]}]

# PadFunction: IO_L5P_T0_34
set_property SLEW FAST [get_ports {DDR3_A[6]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[6]}]
set_property PACKAGE_PIN W1 [get_ports {DDR3_A[6]}]

# PadFunction: IO_L6P_T0_34
set_property SLEW FAST [get_ports {DDR3_A[5]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[5]}]
set_property PACKAGE_PIN U3 [get_ports {DDR3_A[5]}]

# PadFunction: IO_L7N_T1_34
set_property SLEW FAST [get_ports {DDR3_A[4]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[4]}]
set_property PACKAGE_PIN AB1 [get_ports {DDR3_A[4]}]

# PadFunction: IO_L10N_T1_34
set_property SLEW FAST [get_ports {DDR3_A[3]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[3]}]
set_property PACKAGE_PIN AB5 [get_ports {DDR3_A[3]}]

# PadFunction: IO_L10P_T1_34
set_property SLEW FAST [get_ports {DDR3_A[2]}]
```

```
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[2]}]
set_property PACKAGE_PIN AA5 [get_ports {DDR3_A[2]}]

# PadFunction: IO_L8N_T1_34
set_property SLEW FAST [get_ports {DDR3_A[1]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[1]}]
set_property PACKAGE_PIN AB2 [get_ports {DDR3_A[1]}]

# PadFunction: IO_L11N_T1_SRCC_34
set_property SLEW FAST [get_ports {DDR3_A[0]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_A[0]}]
set_property PACKAGE_PIN AA4 [get_ports {DDR3_A[0]}]

# PadFunction: IO_L11P_T1_SRCC_34
set_property SLEW FAST [get_ports {DDR3_BA[2]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_BA[2]}]
set_property PACKAGE_PIN Y4 [get_ports {DDR3_BA[2]}]

# PadFunction: IO_L9P_T1_DQS_34
set_property SLEW FAST [get_ports {DDR3_BA[1]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_BA[1]}]
set_property PACKAGE_PIN Y3 [get_ports {DDR3_BA[1]}]

# PadFunction: IO_L9N_T1_DQS_34
set_property SLEW FAST [get_ports {DDR3_BA[0]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_BA[0]}]
set_property PACKAGE_PIN AA3 [get_ports {DDR3_BA[0]}]

# PadFunction: IO_L12P_T1_MRCC_34
set_property SLEW FAST [get_ports {DDR3_RAS}]
```

```
set_property IOSTANDARD SSTL15 [get_ports {DDR3_RAS}]
set_property PACKAGE_PIN V4 [get_ports {DDR3_RAS}]

# PadFunction: IO_L12N_T1_MRCC_34
set_property SLEW FAST [get_ports {DDR3_CAS}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_CAS}]
set_property PACKAGE_PIN W4 [get_ports {DDR3_CAS}]

# PadFunction: IO_L7P_T1_34
set_property SLEW FAST [get_ports {DDR3_WE}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_WE}]
set_property PACKAGE_PIN AA1 [get_ports {DDR3_WE}]

# PadFunction: IO_L15P_T2_DQS_34
set_property SLEW FAST [get_ports {DDR3_RESET}]
set_property IOSTANDARD LVCMOS15 [get_ports {DDR3_RESET}]
set_property PACKAGE_PIN W6 [get_ports {DDR3_RESET}]

# PadFunction: IO_L14P_T2_SRCC_34
set_property SLEW FAST [get_ports {DDR3_CKE}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_CKE0}]
set_property PACKAGE_PIN T5 [get_ports {DDR3_CKE0}]

# PadFunction: IO_L14N_T2_SRCC_34
set_property SLEW FAST [get_ports {DDR3_ODT}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_ODT}]
set_property PACKAGE_PIN U5 [get_ports {DDR3_ODT}]

# PadFunction: IO_L8P_T1_34
set_property SLEW FAST [get_ports {DDR3_CS[0]}]
```

```
set_property IOSTANDARD SSTL15 [get_ports {DDR3_CS[0]}]
set_property PACKAGE_PIN AB3 [get_ports {DDR3_CS[0]}]

# PadFunction: IO_L4N_T0_35
set_property SLEW FAST [get_ports {DDR3_DM[0]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_DM[0]}]
set_property PACKAGE_PIN D2 [get_ports {DDR3_DM[0]}]

# PadFunction: IO_L8N_T1_AD14N_35
set_property SLEW FAST [get_ports {DDR3_DM[1]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_DM[1]}]
set_property PACKAGE_PIN G2 [get_ports {DDR3_DM[1]}]

# PadFunction: IO_L16N_T2_35
set_property SLEW FAST [get_ports {DDR3_DM[2]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_DM[2]}]
set_property PACKAGE_PIN M2 [get_ports {DDR3_DM[2]}]

# PadFunction: IO_L23N_T3_35
set_property SLEW FAST [get_ports {DDR3_DM[3]}]
set_property IOSTANDARD SSTL15 [get_ports {DDR3_DM[3]}]
set_property PACKAGE_PIN M5 [get_ports {DDR3_DM[3]}]

# PadFunction: IO_L3P_T0_DQS_AD5P_35
set_property SLEW FAST [get_ports {DDR3_DQS_P[0]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_P[0]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_P[0]}]
set_property PACKAGE_PIN E1 [get_ports {DDR3_DQS_P[0]}]

# PadFunction: IO_L3N_T0_DQS_AD5N_35
```

```
set_property SLEW FAST [get_ports {DDR3_DQS_N[0]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_N[0]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_N[0]}]
set_property PACKAGE_PIN D1 [get_ports {DDR3_DQS_N[0]}]

# PadFunction: IO_L9P_T1_DQS_AD7P_35
set_property SLEW FAST [get_ports {DDR3_DQS_P[1]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_P[1]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_P[1]}]
set_property PACKAGE_PIN K2 [get_ports {DDR3_DQS_P[1]}]

# PadFunction: IO_L9N_T1_DQS_AD7N_35
set_property SLEW FAST [get_ports {DDR3_DQS_N[1]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_N[1]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_N[1]}]
set_property PACKAGE_PIN J2 [get_ports {DDR3_DQS_N[1]}]

# PadFunction: IO_L15P_T2_DQS_35
set_property SLEW FAST [get_ports {DDR3_DQS_P[2]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_P[2]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_P[2]}]
set_property PACKAGE_PIN M1 [get_ports {DDR3_DQS_P[2]}]

# PadFunction: IO_L15N_T2_DQS_35
set_property SLEW FAST [get_ports {DDR3_DQS_N[2]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_N[2]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_N[2]}]
set_property PACKAGE_PIN L1 [get_ports {DDR3_DQS_N[2]}]

# PadFunction: IO_L21P_T3_DQS_35
```

```
set_property SLEW FAST [get_ports {DDR3_DQS_P[3]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_P[3]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_P[3]}]
set_property PACKAGE_PIN P5 [get_ports {DDR3_DQS_P[3]}]

# PadFunction: IO_L21N_T3_DQS_35
set_property SLEW FAST [get_ports {DDR3_DQS_N[3]}]
set_property IN_TERM UNTUNED_SPLIT_50 [get_ports {DDR3_DQS_N[3]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_DQS_N[3]}]
set_property PACKAGE_PIN P4 [get_ports {DDR3_DQS_N[3]}]

# PadFunction: IO_L3P_T0_DQS_34
set_property SLEW FAST [get_ports {DDR3_CLKP0}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_CLKP0}]
set_property PACKAGE_PIN R3 [get_ports {DDR3_CLKP0}]

# PadFunction: IO_L3N_T0_DQS_34
set_property SLEW FAST [get_ports {DDR3_CLKN0}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {DDR3_CLKN0}]
set_property PACKAGE_PIN R2 [get_ports {DDR3_CLKN0}]
```